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(54) Method of manufacturing a semiconductor device having a silicon carbide layer.

(57) A method of forming a semiconductor device on a silicon carbide layer (21, 32, 52, 53) comprises steps of selectively introducing an impurity into a selected part (23, 34, 53a, 55c) of the silicon carbide layer, and oxidizing the selected part by annealing the silicon carbide layer in an atmosphere containing oxygen.

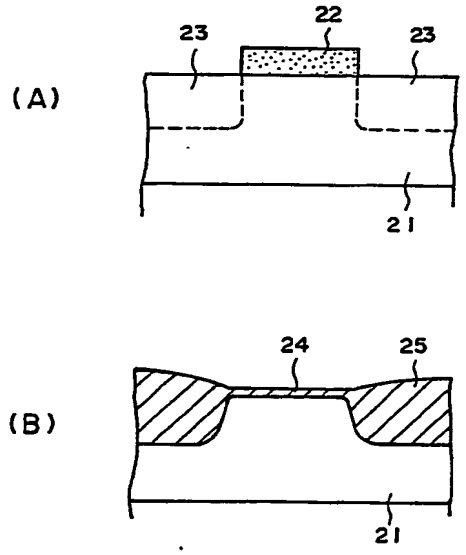

FIG. 2

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METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE HAVING A SILICON CARBIDE LAYER

BACKGROUND OF THE INVENTION

The present invention generally relates to semiconductor devices and more particularly to a method of manufacturing a semiconductor device having a silicon carbide layer.

Silicon carbide is a material having an excellent stability against heat and radiation. Thus, a semiconductor device constructed on a silicon carbide layer is expected to play a major role in electronic instruments to be used in a high temperature and high radioactive environment such as space vehicles, satellites or nuclear reactors.

Conventionally, a semiconductor device constructed on a silicon carbide layer has a problem in that the formation of oxide layer on the a surface of the silicon carbide layer is difficult because of the slow oxidation rate of silicon carbide. Usually, the oxidation rate of silicon carbide is less than one-tenth of that of silicon. Because of this, the technique to form a device isolation structure by thermal oxidation, which is well established in the case of the device constructed on silicon, is not applicable and the semiconductor device has to employ a complex mesa structure in order to achieve a device isolation.

FIGS.1(A) - (C) show a typical prior art process for manufacturing a metal-oxide-silicon field effect transistor (MOSFET) on a silicon carbide layer. Referring to FIG.1(A), a silicon carbide layer 12 is grown on a silicon substrate 11 by chemical vapor deposition, and after deposition of aluminium layer 13 on the silicon carbide layer 12 and a subsequent patterning for exposing the silicon carbide layer 12 except for a device region in which the semiconductor device is to be formed, the structure is etched in a nitrogen trifluoride (NF_3) etching gas and a structure shown in FIG.1(B) is obtained. After the removal of remaining aluminium layer 13, a MOS structure comprising a gate oxide film 14, a gate electrode 15, source and drain regions 16 and 17, and source and drain electrodes 18 are formed by a well known process. Further, an aluminium interconnection 20 is provided on the substrate 11 so as to make a contact with the source and drain electrodes 18 and a MOSFET shown in FIG.1(C) is obtained.

The MOSFET thus obtained, however, has a problem in that the manufacturing process is complex as it involves the step of forming the mesa structure. Further, the integration density is limited because of the separation between the mesa structures. Associated with use of the mesa structure, there arises a further problem in that a leakage current flowing through a side wall of the mesa structure is increased because of minute projections and depressions formed on the side wall at the time of etching. It is believed that such minute projections and depressions facilitate adsorption of impurities on the side wall of the mesa structure and thus provide a path for the leakage current. Furthermore, the steep side wall of the mesa structure tends to cause a disconnection of the metal interconnection 20 particularly at a part 19 along the side wall wh re the thickness of the interconnection is thin. The disconnection of the metal interconnection 20 is facilitated further by the minute projections and depressions on the side wall.

SUMMARY OF THE INVENTION

Accordingly, it is a general object of the present invention to provide a novel and useful method of manufacturing a semiconductor device having a silicon carbide layer, wherein the aforementioned problems are eliminated.

Another and more specific object of the present invention is to provide a method of manufacturing a semiconductor device having a silicon carbide layer, comprising steps of introducing an impurity into a silicon carbide layer in correspondence to a region in which a device isolation structure is to be formed, and selectively oxidizing said region by annealing the device in an atmosphere containing oxygen. According to the present invention, the region in which the impurity is introduced is selectively oxidized and there is formed a thick silicon oxide in correspondence to the device isolation structure. As a result, the hitherto needed mesa structure as well as the patterning and etching processes associated with the formation of the mesa structure can be eliminated and the device is constructed with reduced cost. The planer semiconductor device thus obtained has various advantages such as capability of operating in a high temperature and a high radioactive environment, effective device isolation, high integration density, low leakage current, and easy construction of a multi-level interconnection structure.

Other objects and further features of the present invention will become apparent from the following detailed description when read in conjunction with attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS.1(A) - (C) are diagrams showing various steps for manufacturing a prior art semiconductor device constructed on a silicon carbide layer;

FIGS.2(A) and (B) are diagrams for explaining the principle of the present invention;

FIG.3 is a graph showing oxidation of silicon carbide doped with boron with various dos s as a function of time;

FIGS.4(A) - (E) are diagrams showing various steps of manufacturing a MOSFET on a silicon carbide layer; and

FIGS.5(A) - (E) are diagrams showing various steps of manufacturing a bipolar transistor on a silicon carbide layer.

DETAILED DESCRIPTION

FIGS.2(A) and (B) show the principle of the present invention. Referring to FIG.2(A), a part of a silicon carbide substrate 21 on which a semiconductor device is to be formed is covered by a photoresist 22 and an impurity such as phosphorus (P), boron (B), arsenic (As) or compound of these elements is introduced into an uncovered part of the silicon carbide substrate. As a result, an impurity region 23 doped with the impurity is formed. Further, the photoresist 22 is removed and the structure of FIG.2(A) is subjected to thermal oxidation.

FIG.3 shows a result of experiment conducted to evaluate the oxidation rate of silicon carbide doped to various dopant concentration levels. The experiment was conducted on a specimen of silicon carbide in which B is introduced by ion implantation with an acceleration voltage of 80 keV. The specimen was further heat treated in a reaction vessel (not shown) under an atmosphere containing oxygen at 1050 °C. Th oxygen partial pressure was controlled by flowing oxygen and hydrogen into the reaction vessel such that there is established a water vapor pressure of 760 Torr in the reaction vessel. In the drawing, the curve I represents a case in which boron ion (B^+) is introduced by ion implantation with a dose of 5×10^{12} cm^{-2}, the curve II represents a case in which the dose is 1×10^{14} cm^{-2}, and the curve III represents a case in which the dose is 1×10^{15} cm^{-2}. As can be clearly seen from the drawing, the rate of oxidation, represented by the thickness of silicon oxide film grown on the silicon carbide, is increased with increasing concentration of B in the specimen. The thickness of the silicon oxide film after the heat treatment for one hour is summarized in the following Table I.

TABLE I

relation between oxidation rate and dose of boron in silicon carbide	
dose (cm^{-2})	SiO_2 thickness (nm)
5×10^{12}	20
1×10^{14}	100
1×10^{15}	250

Generally, it was found that the oxidation rate of undoped or pure silicon carbide measured in the temperature range of 950 - 1150 °C is only about 4 - 8 % of that of silicon while when the impurity such as B, P, As or compound of these elements is introduced with a concentration level of more than about 1×10^{19} cm^{-3}, the oxidation rate increases to as much as 40 -60 % of that of silicon.

Thus, as a result of heat treatment of the structure of FIG.2(A) for a limited duration, a thick xide layer 25 is formed in the impurity region 23 because of the increased oxidation rate. On the other hand, there is formed only a thin oxide layer 24 in the part of the substrate 21 on which the device is to be form d. In one example, an oxide layer having a thickness of 400 - 800 nm and a breakdown voltage of 6 -10 MV/cm is obtained by oxidation for two through four hours. Using the technique disclosed herein, one can construct a

planer semiconductor device constructed on a silicon carbide substrate and the problems associated with the prior art semiconductor device can be successfully eliminated.

Next, the present invention will be described in more detail with respect to a first embodiment with reference to FIGS.4(A) - (E). In this embodiment, the semiconductor device is a MOSFET.

Referring to FIG.4(A), a layer 32 of β- phase silicon carbide (referred to hereinafter as β-SiC) is grown on a (111) surface of an n-type silicon substrate 31 having a resistivity of 1 - 10 Ω-cm by chemical vapor deposition. In one example, the growth is made by introducing trichlorosilane ($SiHCl_3$) and propane (C_3H_8) into a reactor (not shown) as source gases. As the $SiHCl_3$ is supplied in a form of liquid, the introduction of the source gas is performed by bubbling using hydrogen (H_2). The growth is made at a reduced pressure of 3.0 Torr and a temperature of 1000° C. The flow rate of $SiHCl_3$, C_3H_8 and H_2 is adjusted such that the partial pressure of $SiHCl_3$, C_3H_8 and H_2 are respectively 3.57×10^{-4} Torr, 1.53×10^{-5} Torr, and 3.57×10^{-3} Torr. At the time of growth of the silicon carbide layer 32, a diborane (B_2H_6) gas is added to the source gas so that the obtained silicon carbide layer 32 is doped to the p-type and has a resistivity of 1 - 10 Ωcm.

Next, a photoresist 33 is applied on the SiC layer 32 in correspondence to a region in which the semiconductor device is to be formed and the structure thus obtained is subjected to ion implantation of phosphorus ion (P^+) using the photoresist 33 as a mask. The ion implantation is made under an acceleration voltage of 80 - 120 keV with a dose of 10^{14} - 10^{15} cm^{-2} and thus an impurity region 34 is formed in correspondence to the device isolation structure as shown in FIG.4(B).

After the removal of the photoresist 33, the structure of FIG.4(B) is oxidized in a thermal oxidation furnace at 1050° C for two hours under one atmosphere while flowing oxygen and hydrogen such that the partial pressure of water vapor (H_2O) formed in the furnace is maintained at about 760 Torr. As a result, as illustrated in FIG.4(C), a thin oxide layer 35 is formed in correspondence to the region protected by the photoresist against ion implantation. On the other hand, there is formed a thick oxide layer 36 in correspondence to the impurity region 34 with a thickness of about 400 - 600 nm.

Next, a polysilicon layer is deposited on the thin oxide layer 35 and after suitable patterning to form a gate electrode 37 as shown in FIG.4(D), a source region 38 and a drain region 39 are formed by ion implantation of P^+ using the gate electrode 37 as well as the thick oxide layer 36 as the mask. Further, the surface of the gate electrode 37 is oxidized and an oxide film 40 covering the gate electrode 37 is formed.

Further, a phosphosilicate glass (PSG) layer 41 is deposited on the structure of FIG.4(D) as an interlayer insulator and contact holes are provided on the PSG layer 41 as well as on the silicon oxid layers 35 and 40 existing under the layer 41, in correspondence to the source region 38, drain region 39 and the gate electrode 37. After deposition of aluminium layer 42 on the PSG layer 41 in contact with th regions 38 and 39 as well as in contact with the gate electrode 27 and subsequent patterning, the MOSFET shown in FIG.4(E) is completed.

According to the present invention, the oxidation rate of the SiC 32 is selectively enhanced by introducing the impurity with a large dosage and the thick oxide layer 35 is formed exactly in correspondence to the device isolation structure. Further, by changing the energy of ion implantation, the thickness of the oxide layer 35 is controlled easily. As the MOSFET obtained by the process of the present inv ntion has the planer structure, the step of providing the mesa structure as well as the step for obtaining a flat top surface suitable for interlayer connection is eliminated and the manufacturing process is significantly simplified. Associated therewith, the degree of integration can be increased and the leakage current is minimized.

Next, a second embodiment of the present invention will be described with reference to FIGS.5(A) - (E). In this embodiment, the semiconductor device is a bipolar transistor.

In this embodiment, an n^+-type β-SiC layer 52 and an n-type β-SiC layer 53 are grown successively on a silicon substrate 51 similarly to the first embodiment with a thickness of 3000 Å for the layer 52 and 2000 Å for the layer 53. During the growth of the layers 52 and 53, phosphine (PH_3) is added to the source gas with a partial pressure of 1.02×10^{-8} Torr and a partial pressure of 1.53×10^{-10} Torr respectively so that th layer 52 and the layer 53 are doped to a carrier concentration level of 5×10^{18} cm^{-3} and 1×10^{17} cm^{-3}. Next, a photoresist 54 is applied on the layer 53 and subsequently patterned so as to expose a part 53a of the SiC layer 53 corresponding to the device isolation structure to be formed. FIG.5(A) shows a structure obtained by the foregoing procedures.

Next, B^+ is introduced to the exposed part 53a of the SiC layer 53 by ion implantation under an acceleration voltage of 400 keV with a dose of about $5 \times 10^{14}/cm^{-2}$ to about $1 \times 10^{15}/cm^{-2}$. Further, the structure thus processed is ann aled at 1100° C, one atmosphere with a H_2O partial pressure of 760 Torr and a device isolation oxide lay r 55 is formed. Note that the device isolation oxide layer 55 thus formed includes a large thickness region 55a having a thickness corresponding to the total thickness of the SiC

layers 52 and 53 at the region in which the ion implantation of B^+ is made and a small thickn ss region 55b in correspondence to th region in which the ion implantation is not made. The structure thus obtained is further applied with a photoresist 56 which is subsequently patterned so as to expose a part 55c of the thin oxide region 55b at both sides of the emitter to be formed in the structure. Thus, a structure shown in FIG.5(B) is obtained.

After injecting B^+ under an acceleration voltage of 100 keV with a dose of 5×10^{14} - 1×10^{15} cm^{-2}, the structure of FIG.5(C) is heat treated similarly to the foregoing case and a pair of oxide regions 55d as shown in FIG.5(C) are formed.

The structure of FIG.5(C) is further deposited with a thin silicon nitride layer 57 by chemical vapor deposition and a part of the layer 57 corresponding to the emitter and the base of the bipolar transistor is selectively removed by etching. After the etching, a part of the silicon oxide layer 55b underlying the removed part of the layer 57 is further etched and a p-type β-SiC layer 58 is subsequently grown so as to make a contact with a part of the SiC layer 53 exposed by the foregoing etching process for a thickness of about 500 - 1000 Å. The growth of the SiC layer 58 is performed similarly to the case of growing the layers 52 and 53 except that B_2H_6 or trimethyl boron is added to the source gas such that the SiC layer 58 is doped to the p-type with a hole concentration level of about 5×10^{19} cm^{-3}. For this purpose, the partial pressure of B_2H_6 is set to $1 - 5 \times 10^{-7}$ Torr. When trimethyl boron is used, the partial pressure is set to $3 - 5 \times 10^{-8}$ Torr. The SiC layer 58 is further removed selectively by plasma etching using nitrogen trifluoride NF_3 so that only a part of the layer 58 corresponding to the base of the bipolar transistor and making a direct contact with the exposed part of the SiC layer 53 is left as illustrated in FIG.5(D).

Further, a silicon oxide layer 59 is deposited on the structure of FIG.5(D) by chemical vapor deposition and a contact hole 59a is provided so as to expose the foregoing part of the SiC layer 58 in contact with the layer 53. After the contact hole 59a is formed, an n^+-type SiC layer 60 is grown on the SiC layer 58 in correspondence to the contact hole 59a for a thickness of about 2000 Å by a process similar to that used for growing the layers 52 and 53, except that the partial pressure for PH_3 is set to 1.02×10^{-7} Torr so that a carrier concentration level of about 5×10^{19} cm^{-3} is obtained. The layer 60 is then patterned so that only a part thereof corresponding to the emitter of the transistor is left on the part of the layer 58 making a direct contact with the underlying SiC layer 53. Further, after formation of the contact holes 59b and 59c for the base and emitter of the bipolar transistor, aluminium is deposited so as to fill the contact holes 59a - 59c and the bipolar transistor is completed.

In this process, too, the selective oxidation of SiC facilitates the formation of the device isolation structure. Thus, the bipolar transistor can be formed by a simple procedure without providing the mesa structure.

Although the process for introducing the impurity into the silicon carbide layer described heretofore is ion implantation, the present invention is not limited as such but solid diffusion process or vapor phase diffusion process can be employed similarly for this purpose. Further, the impurity to be introduced into silicon carbide for selective oxidation is not limited to B and P, but As may be used with substantially a same result. The substrate 21, 31 or 51 is not limited to silicon single crystal but may be a bulk silicon carbide or a silicon epitaxial layer grown of an insulator such as sapphire.

Further, the present invention is not limited to these embodiments but various variations and modifications may be made without departing from the scope of the invention.

Claims

1. A method of forming a semiconductor device on a silicon carbide layer (21, 31, 52, 53), characterized by steps of selectively introducing an impurity into a selected part (23, 34, 53a, 55c) of the silicon carbide layer, and oxidizing said silicon carbide layer by annealing in an oxidizing atmosphere.

2. A method as claimed in claim 1, characterized in that said impurity is selected from a gr up of elements comprising boron, phosphorus and arsenic.

3. A method as claimed in claim 1 or 2, characterized in that said impurity is introduced with a concentration level sufficient to cause a selective oxidation in said part (23, 34, 53a, 55c) of the silicon carbide layer (21, 32, 52, 53) in which the impurity is introduced when annealed in said step of oxidizing.

4. A method as claimed in claim 1, 2 or 3, characterized in that said impurity is introduc d with a concentration level of about 1×10^{19} cm^{-3} or more.

5. A method as claimed in claim 1, 2, 3 or 4, characterized in that said impurity is introduced into th silicon carbide layer (21, 32, 52, 53) by ion implantation.

6. A method as claimed in claim 5, characterized in that said ion implantation is made with a dose of

about 10^{14} - 10^{15} cm^{-2}.

7. A method as claimed in anyone of claims 1 to 6, characterized in that said annealing is performed at a temperature ranging from 950° C - 1150° C.

8. A method as claimed in anyone of claims 1 to 7, characterized in that said silicon carbide layer (32, 52) is formed on a single crystal silicon (31, 51).

9. A method as claimed in anyone of claims 1 to 7, characterized in that said silicon carbide layer (32, 52) is formed on a silicon carbide bulk crystal (31, 51).

10. A method as claimed in anyone of claims 1 to 7, characterized in that said silicon carbide layer (32, 52) is formed on a silicon layer (31, 51) grown on an insulator.

11. A method as claimed in anyone of claims 1 to 10, characterized in that said step of selectively introducing the impurity comprises a step of masking the silicon carbide layer (32, 52, 53) according to a predetermined pattern such that a plurality of device isolation regions (34, 53a, 55c) are selectively exposed as said selected part of the silicon carbide layer and a step of introducing the impurity into said plurality of device isolation regions, and said step of oxidizing comprises a step of forming an oxide isolation structure (36, 55a, 55d) in correspondence to the device isolation region and an oxide layer (35, 55b) covering the device isolation region with a thickness substantially smaller than that of the oxide isolation structure.

12. A method as claimed in claim 11, characterized in that the method further comprises a step of forming the semiconductor device on a device region defined between said plurality of device isolation regions (34, 53a, 55c) after the step of oxidizing.

13. A method as claimed in claim 12, characterized in that said step of forming the semiconductor device comprises a step of providing a gate electrode (37) on a part of the oxide layer (35) covering said device region and a step of introducing an impurity into said device region by ion implantation using the gate electrode as a mask.

14. A method as claimed in claim 12 characterized in that said step of forming the semiconductor device comprises a step of exposing the silicon carbide layer (53) at a part of the device region by removing the oxide layer (55b) therefrom, depositing a second silicon carbide layer (58) with a conduction type opposite to that of the first silicon carbide layer so as to make a direct contact with the exposed part of the first silicon carbide layer, and depositing a third silicon carbide layer (60) with a conduction type identical to that of the first silicon carbide layer so as to make a direct contact with a part of the second silicon carbide layer.

15. A method of forming an oxide layer on a silicon carbide layer characterized by steps of selectiv ly introducing an impurity into a selected part of the silicon carbide layer, and oxidizing the silicon carbide layer by annealing in an oxidizing atmosphere.

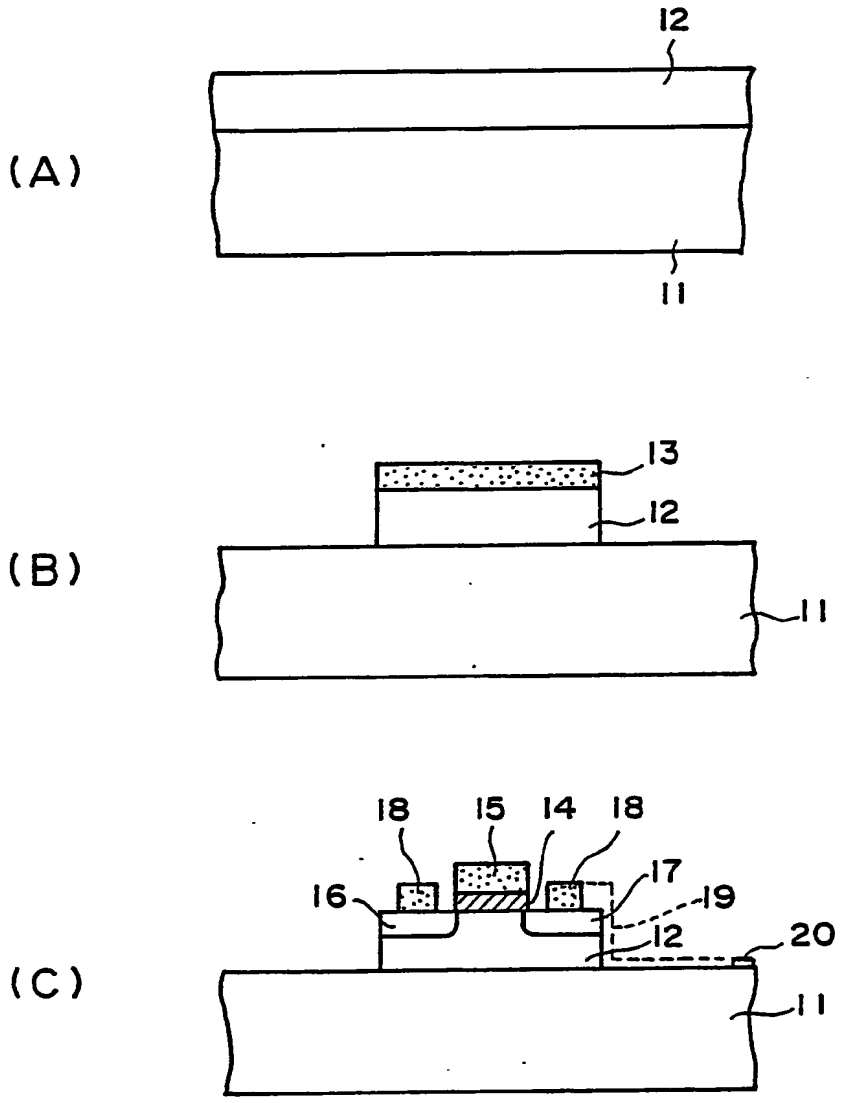


FIG. 1
PRIOR ART

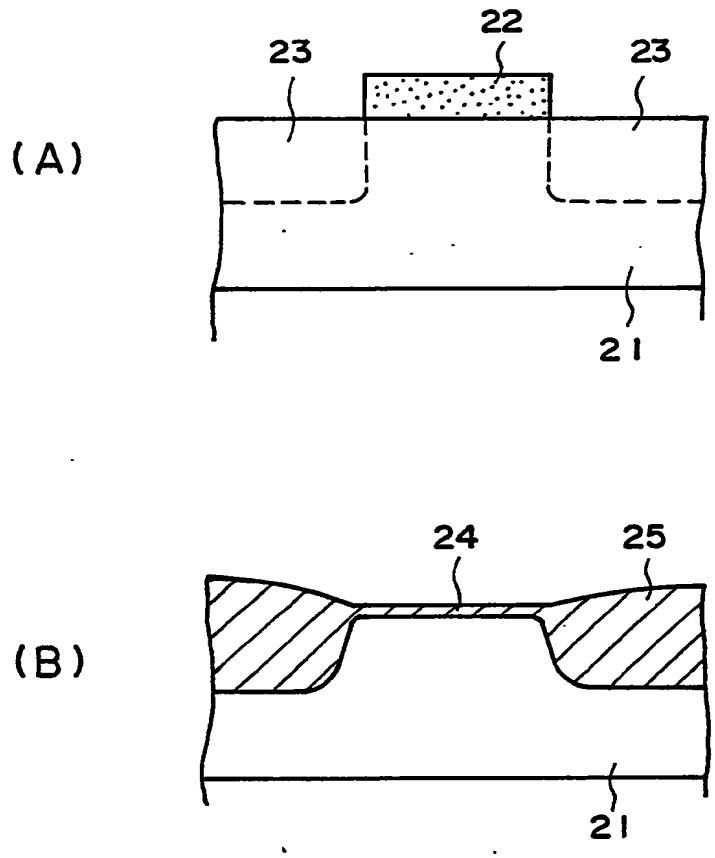


FIG. 2

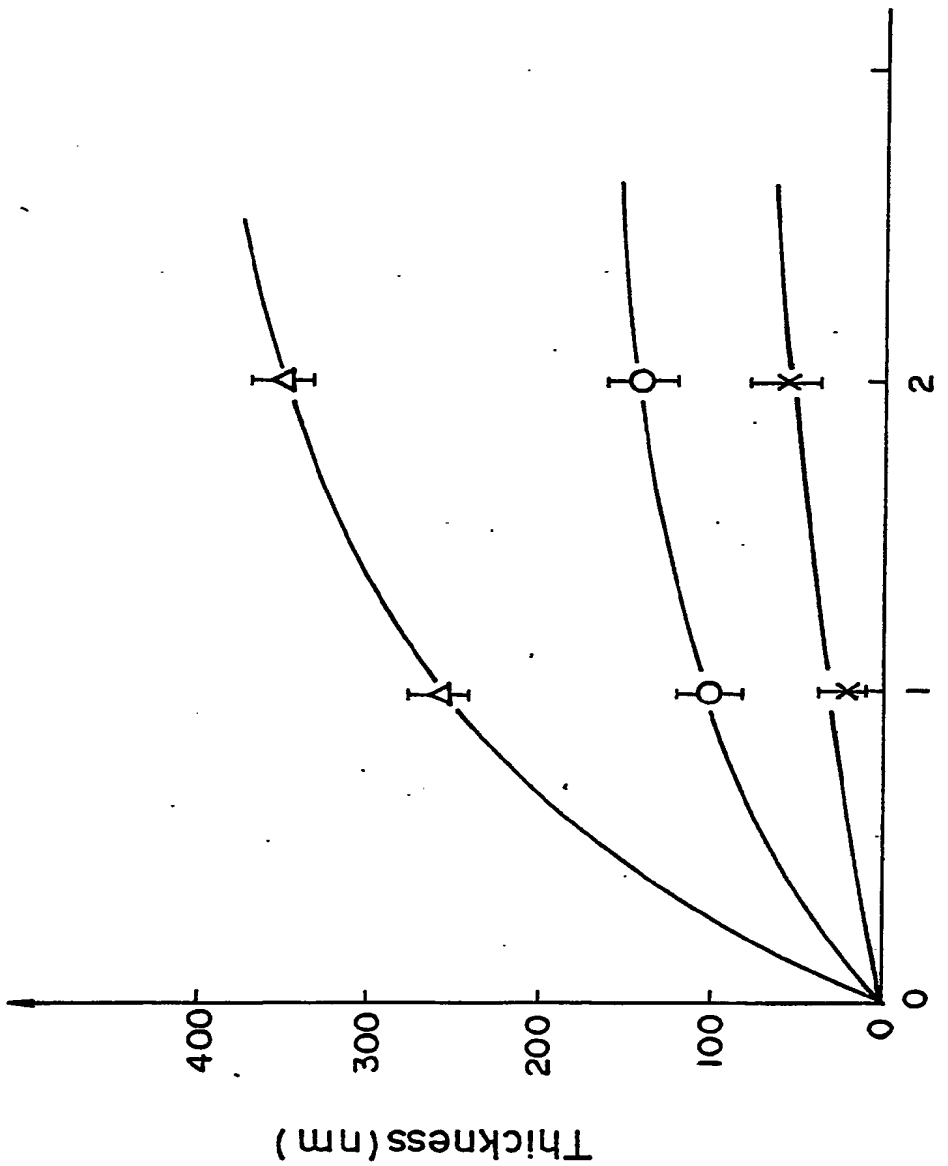


FIG. 3

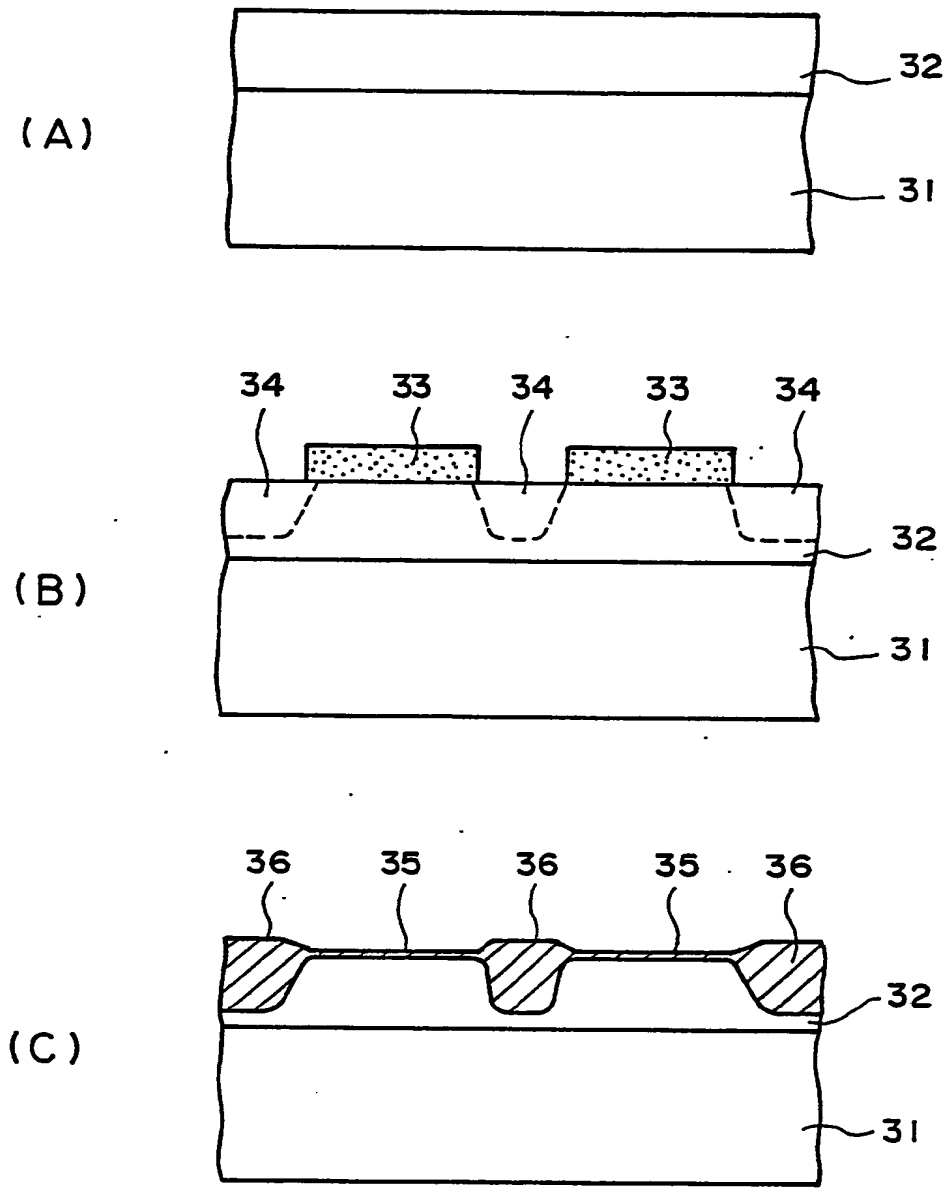
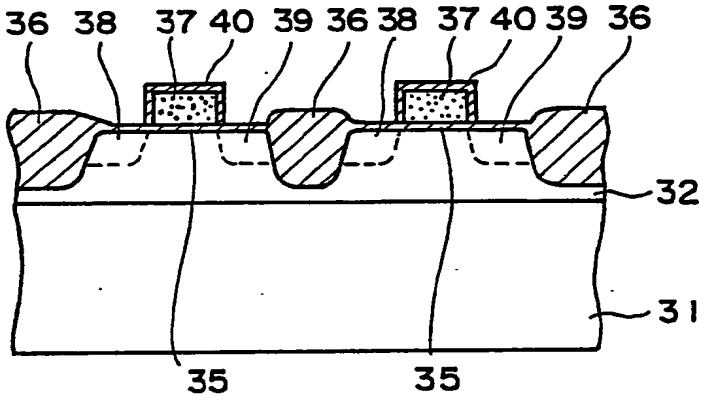


FIG. 4

(D)



(E)

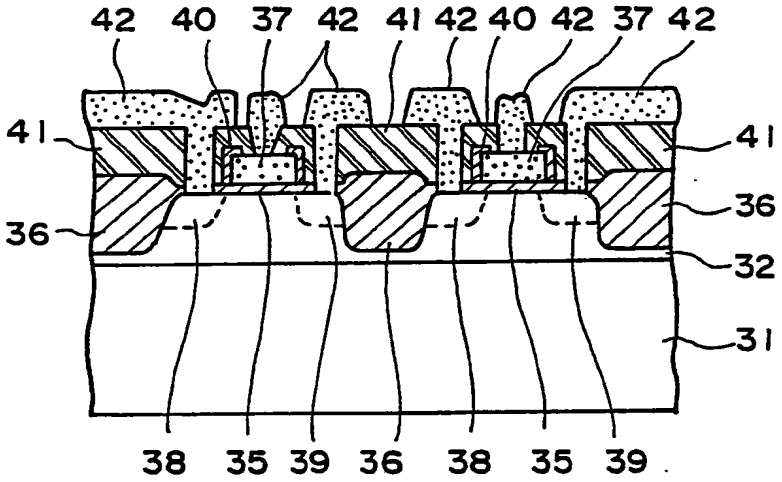


FIG. 4

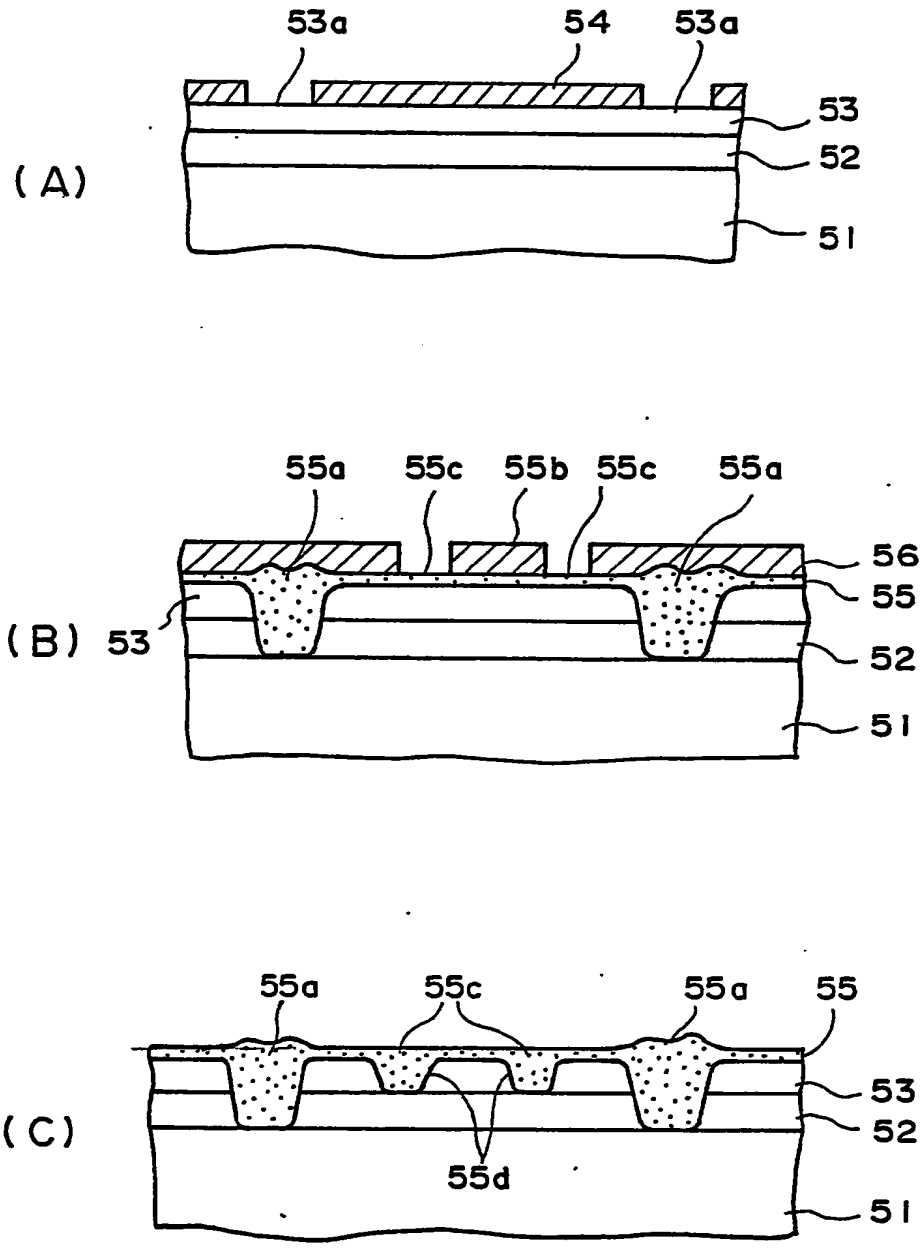


FIG. 5

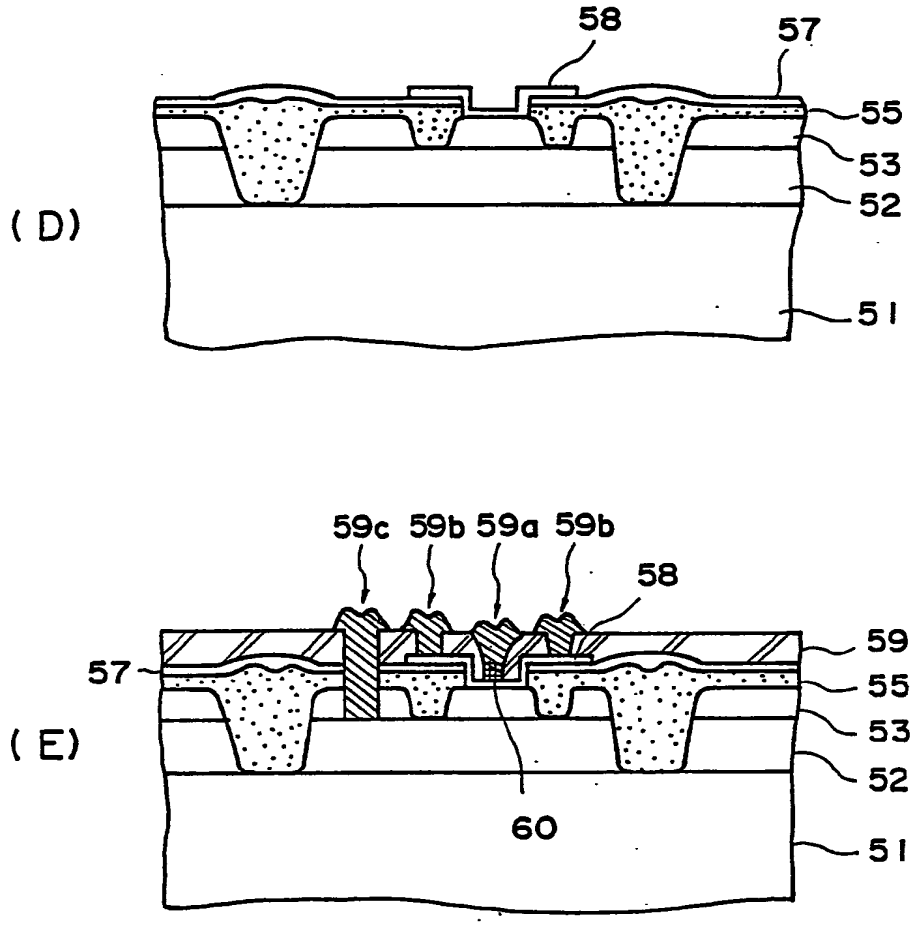


FIG. 5

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 89 11 8919

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	IEEE ELECTRON DEVICE LETTERS, vol. EDL-7, no. 12, December 1986, pages 692-693, IEEE, New York, US; K. SHIBAHARA et al.: "Fabrication of inversion-type n-channel MOSFET's using cubic-SiC on Si(100)" * Whole article * ---	1,2,4-9 ,15	H 01 L 21/473 H 01 L 21/82
A	US-A-4 757 028 (AGENCY OF IND. SCIENCE AND TECHNOLOGY) * Whole document * ---	1-15	
A	DE-A-3 446 961 (SHARP) * Figure 1G; page 7 * -----	14	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21-11-1989	SINEMUS M.

CATEGORY OF CITED DOCUMENTS

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